relationship with at least one of said scanning electrode, said signal electrode and a thin film transistor for enabling driving of the liquid crystal display apparatus in a reflection type display mode.

as concl.

26. A liquid crystal display apparatus according to claim 25, wherein said liquid crystal layer is a guest-host type liquid crystal.--

REMARKS

By the above amendment, the status of the parent application has been updated to indicate the patent number thereof, minor informalities in the specification have been corrected, independent claims 1 and 10 have been amended to clarify features thereof, with claims 2-5, 8, 12, 13 and 15-17 being canceled, dependent claims being amended and new claims 18-26 being presented, wherein claim 18 is an independent claim corresponding somewhat to previous independent claim 15.

Applicants note that this amendment is submitted within two months of the date of the Office Action dated November 29, 2002, and note that this response is the first substantive response to an outstanding Office Action in this application.

As to the rejection of claims 1-17 under the judicially created doctrine of double patenting over claims 1-24 of U.S. Patent No. 6,115,017, the patent issuing from the parent application in this application, as recognized by the Examiner, such rejection can be overcome by the submission of a Terminal Disclaimer. Applicants, without acquiescing in the propriety of the double patenting rejection as set forth, in order to expedite the prosecution of this application, submit herewith a Terminal Disclaimer and the appropriate fee therefor. Accordingly, applicants submit that this rejection should now be overcome.

As to the rejection of claims 1, 2, 5-10 and 12-17 under 35 U.S.C. 102(b) as being anticipated by Hamada et al (US 5,194,974) and the rejection of claims 3, 4 and 11 under 35 U.S.C. 103(a) as being unpatentable over Hamada et al (US

5,194,974) in view of Yamaguchi et al (US 5,627,557), such rejections are traversed insofar as they are applicable to the present claims, and reconsideration and withdrawal of the rejections are respectfully requested.

At the outset, as to the requirements to support a rejection under 35 U.S.C. 102, reference is made to the decision of In re Robertson, 49 USPQ 2d 1949 (Fed. Cir. 1999), wherein the court pointed out that anticipation under 35 U.S.C. §102 requires that each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. As noted by the court, if the prior art reference does not expressly set forth a particular element of the claim, that reference still may anticipate if the element is "inherent" in its disclosure. To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Moreover, the court pointed out that inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.

With regard to the requirements to support a rejection under 35 U.S.C. 103, reference is made to the decision of In re Fine, 5 USPQ 2d 1596 (Fed. Cir. 1988), wherein the court pointed out that the PTO has the burden under §103 to establish a prima facie case of obviousness and can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. As noted by the court, whether a particular combination might be "obvious to try" is not a legitimate test of patentability and obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. As further noted by the court, one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.

Furthermore, such requirements have been clarified in the recent decision of In re Lee, 61 USPQ 2d 1430 (Fed. Cir. 2002) wherein the court in reversing an obviousness rejection indicated that deficiencies of the cited references cannot be remedied with conclusions about what is "basic knowledge" or "common knowledge". The court pointed out:

> The Examiner's conclusory statements that "the demonstration mode is just a programmable feature which can be used in many different device[s] for providing automatic introduction by adding the proper programming software" and that "another motivation would be that the automatic demonstration mode is user friendly and it functions as a tutorial" do not adequately address the issue of motivation to combine. This factual question of motivation is immaterial to patentability, and could not be resolved on subjected belief and unknown authority. It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to "[use] that which the inventor taught against its teacher."... Thus, the Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion. (emphasis added)

Turning to claim 1, applicants note that irrespective of the Examiner's position concerning the applicability of Hamada et al to such claim, by the present amendment, claim 1 has been amended to recite the feature that "the display data holding circuit having one of a coplanar and an inverse stagger structure". As described at page 15, lines 13-15 of the specification, "Figs. 5 to 7 show examples of application to a TFT with a coplanar structure" and as indicated at page 17, lines 15-18, as amended, "Fig. 8 shows the configuration of the mask for the pixel portion with an inverse stagger structure, and Fig. 9 shows the cross section of A-B-C-D-E portions of the inverse stagger structure shown in Fig. 8.". While the Examiner refers to the display data holding circuit of Hamada et al as including TFT 1 and C1, applicants submit that Hamada et al merely discloses an amorphous Si TFT and fails to disclose a TFT of the inverse stagger structure or coplanar structure as disclosed

and claimed. Applicants note that such structural arrangement provide an improved structure and operation as described in the specification of this application, which features are not disclosed by Hamada et al in the sense of 35 U.S.C. 102 or rendered obvious in the sense of 35 U.S.C. 103. Applicants note that any attempt to suggest that such features could be utilized in Hamada et al represents a hindsight reconstruction attempt of the present invention utilizing the principle of "obvious to try" which is not the standard of 35 U.S.C. 103. See In re Fine, supra. Thus, applicants submit that claim 1, as amended, patentably distinguishes over Hamada et al in the sense of 35 U.S.C. 102 and 35 U.S.C. 103, and claim 1 and its dependent claims should be considered allowable thereover.

With respect to the dependent claims, applicants note that claim 6 has been amended to recite the feature of a capacitor at least partially formed by a portion of one of the drain and the source of the thin film transistor. Applicants note that in Fig. 7 of the coplanar structure and Fig. 9 of the inverse stagger structure, the capacitor is represented by reference numeral 11 and is formed by one of the drain and source 54 of TFT 10 in Fig. 7 and 19 of TFT 10 in Fig. 9 as described at page 17, lines 5-7 and 20-22. Applicants submit that such features are not disclosed or taught by Hamada et al in the sense of 35 U.S.C. 102 or 35 U.S.C. 103, and claim 6 and its dependent claims patentably distinguish over this cited art and should be considered allowable thereover.

With respect to claim 7 which depends from claim 6, such claim recites further features and applicants note that due to the structural arrangement, as recited, a connection is established through a layer having a potential equal to that of the electrode forming the capacitor. Hereagain, such features are not disclosed or taught by Hamada et al, such that claim 7 should be considered allowable.

As to claim 9, this claim which depends from claim 1 and recites further features of the present invention, has been amended to recite the feature of a static memory circuit, which static memory circuit includes a plurality of thin film transistors

in the memory circuit 13 as illustrated in Fig. 4. Hereagain, such features are not disclosed or taught by Hamada et al, such that this claim should also be considered to patentably distinguish thereover.

As to claim 10, such claim is an independent claim and is generally directed to the liquid crystal display apparatus as illustrated in Fig. 12 of the drawings of this application. Applicants note that in accordance with Fig. 12, a feature of the pixel circuit is that the scanning lines are in a matrix structure, wherein a circuit consisting of a first TFT 25 and a second TFT 24 is incorporated in the pixel for selection per pixel to achieve dot sequential scan. While the Examiner refers to Fig. 5 of Hamada et al, applicants note that Hamada et al fails to show a construction for performing selection per pixel. That is, in Hamada et al, Y1 and Y2 are scanning lines and in accordance with Fig. 4 thereof, one end of the memory capacitor C1 is connected to the reference voltage line E, whereas in Fig. 5 of Hamada et al, one end of the memory capacitor is connected to the scanning line Y2 of the adjacent row. Thus, Hamada et al discloses a line sequential scan, in which selection is made per row. Applicants note that Figs. 45 and 47 of this application illustrate a circuit construction, wherein AND logic of first and second scanning lines is employed in each individual pixel for permitting selection per pixel. Furthermore, applicants note that claim 10 has been amended to recite the feature that a drive voltage of the liquid crystal display apparatus is an alternating current voltage having a period which is shorter than a period of fetching by the display data holding circuit. Referring to Fig. 13 of the drawings of this application, the period of the driving voltage is considered to be represented by Vlcd, whereas the period of the fetching by the display data holding circuit is considered to be represented by Vmem and applicants submit that such features are not disclosed in the sense of 35 U.S.C. 102 or rendered obvious in the sense of 35 U.S.C. 103 from the disclosure and teaching of Hamada et al, such that claim 10 and its dependent claims should be considered to patentably distinguish thereover and considered allowable at this time.

Applicants note that the Examiner has cited Yamaguchi et al in combination with Hamada et al in relation to dependent claim 11 in recognizing that Hamada et al do not disclose an AC voltage generation means for generating a liquid crystal drive voltage and other features. Assuming arguendo that Yamaguchi et al may be considered to disclose an AC voltage generation means for generating a liquid crystal drive voltage, it is readily apparent that Yamaguchi et al does not overcome the deficiencies of Hamada et al with regard to the claimed features of claim 10 in relation to the period of the drive voltage and the period of fetching by the display data holding circuit. Thus, applicants submit that claim 10, as amended, and dependent claims therefrom patentably distinguish over Hamada et al taken alone or in combination with Yamaguchi et al in the sense of 35 U.S.C. 103 and should be considered allowable thereover.

With respect to dependent claim 14 which depends from claim 10, such claim more particularly defines the data holding circuit and the pixel selection circuit consisting of the first and second TFTs 24 and 25 as illustrated in Fig. 12, for example, and such claim which is now dependent upon claim 10, further patentably distinguishes over the cited art in the sense of 35 U.S.C. 103 and should be considered allowable thereover.

As to newly added independent claim 18 which is a clarification of claim 15, recites in the manner similar to that of claim 1, as amended, a display data holding circuit having one of an inverse stagger structure and a coplanar structure, while reciting further features of the present invention. Applicants note that dependent claims 19 and 20 recite additional features of the present invention, which are not disclosed or taught by Hamada et al taken alone in the sense of 35 U.S.C. 102 or 35 U.S.C. 103 or in combination with Yamaguchi et al in the sense of 35 U.S.C. 103. Applicants note that in Hamada et al, mutually opposite phases are applied to the counter electrode and the common electrode and the common electrode so as to directly drive the liquid crystal by the switching device. Claim 18, however, provides

a structural arrangement in which the same phase of the alternating current voltage is applied to the counter electrode and the common electrode and a reference voltage which is substantially a direct current voltage is applied to a reference electrode. In the non-illuminating pixel, the common line and the display electrode are configured so as to make the potential equal to the counter electrode so as to not apply the voltage to be applied, and in the illuminating pixel, the voltage of the reference electrode is applied to the display electrode for a short period immediately before reversal or inversion of polarity to charge a voltage difference with the counter electrode and isolate the display electrode so as to be placed in a floating condition after reversal for holding the voltage and to make the polarity of the voltage of the display electrode substantially an opposite phase of the voltage of the counter electrode. Such features as recited in claims 18-20 are not disclosed or taught by Hamada et al taken alone or in combination with Yamaguchi et al. Furthermore, while the Examiner has contended that Hamada et al disclose an n-channel and a p-channel TFT, applicants submit that Hamada et al only discloses amorphous TFT of nch type and applicants submit that P·CVD, n+a·Si in Hamada et al does not represent pch. Applicants note that with the present invention, driving is effected which enables lowering of power consumption and such features as recited in claims 18-20 are not disclosed or taught in the cited art, and such claims further patentably distinguish over Hamada et al taken alone or in combination with Yamaguchi et al and such claims should be considered allowable thereover.

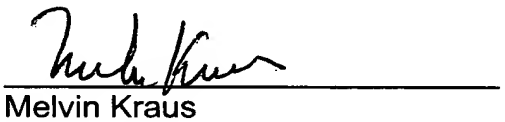
With respect to newly added claims 21-26, applicants note that such claims further define the feature of an opaque reflection electrode arranged in overlapping relationship with at least one of the scanning electrode, the signal electrode and a thin film transistor for enabling driving of the liquid crystal display apparatus in a reflection type display mode as illustrated in Fig. 20 of the drawings of this application, as described at pages 31-33, for example, with the dependent claims also defining the liquid crystal layer as being a guest host type liquid crystal as

described at page 33, lines 6-8, for example. Hereagain, such features are not disclosed or taught in the cited art, such that these dependent claims should be considered allowable together with the parent claims.

In view of the above amendments and remarks, applicants submit that all claims now present in this application patentably distinguish over the cited art, and should now be in condition for allowance. Accordingly, issuance of an action of a favorable nature is courteously solicited.

To the extent necessary, applicant's petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (503.35282CX2) and please credit any excess fees to such deposit account.

Respectfully submitted,



Melvin Kraus
Registration No. 22,466
ANTONELLI, TERRY, STOUT & KRAUS, LLP

MK/cee
(703) 312-6600

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Page 1, please amend the paragraph beginning at line 3 as follows:

CROSS REFERENCE TO RELATED APPLICATION

This is a continuation of U.S. application Serial No. 08/820,835, filed March 19, 1997, now U.S. Patent No. 6,115,017, the subject matter of which is incorporated by reference herein.

Page 15, please amend the paragraph beginning at line 5 as follows:

It is possible to form a two-layer-wiring in the pixel with a display data holding circuit. Therefore, if it is possible to employ a multi-layer wiring technique to do the inter-layer connecting and form a capacitor and a TFT, the above-mentioned pixel can apply to any structures, such as the existing p-Si coplanar structure, inverse-~~Stagger~~ stagger structure and ~~Stagger~~ stagger structure.

Page 17, please amend the paragraph beginning at line 15 as follows:

~~Figs.~~ Fig. 8 shows the configuration of the mask for the pixel portion with an inverse stagger structure, and Fig. 9 shows the cross section of A-B-C-D-E portions of the inverse stagger structure shown in Fig. 8. Because of the inverse stagger structure, the gate electrode 18 of the TFT exists on the lowest layer. The sampling capacitor 11 is formed between the common electrode 8 and the source electrode 19 of the sampling capacitor. By adopting such a structure, the insulating film of the sampling capacitor can be commonly used with a protection insulating film 57 of the sampling TFT. Therefore, it is possible to simplify the manufacturing process, making it suitable for a mass production in the currently main product.

IN THE CLAIMS:

Please amend claim 1 as follows:

1. (amended) A liquid crystal display apparatus having a pair of substrates of which at least one substrate is transparent and a liquid crystal layer sandwiched between the substrates, comprising:

a plurality of scanning electrodes formed on one of the substrates; and

a plurality of signal electrodes intersecting in a matrix form with said plurality of scanning electrodes;

wherein the display apparatus further comprises, within each of the regions surrounded by said plurality of scanning electrodes and said plurality of signal electrodes:

(a) a display data holding circuit connected to a corresponding scanning electrode and signal electrode, for fetching and storing display data from a signal electrode in response to a scanning signal for holding a display image without updating the display data while a power supply to the display apparatus is maintained, the display data holding circuit having one of a coplanar and an inverse stagger structure;

(b) a switching device connected to said display data holding circuit and having a switching operation thereof controlled by the display data holding circuit; and

(c) a display electrode connected to said switching device.

Please cancel claims 2-5 without prejudice or disclaimer of the subject matter thereof.

Please amend claim 6 as follows:

6. (amended) A liquid crystal display apparatus according to claim 1, wherein said display data holding circuit includes a thin film transistor having a gate

connected to the corresponding scanning electrode and one of a drain and a source connected to the corresponding signal line, and a capacitor ~~connected to the other~~ at least partially formed by a portion of one of the drain and the source of said thin film transistor.

Please cancel claim 8 without prejudice or disclaimer of the subject matter thereof.

Please amend claims 9-11 as follows:

9. (amended) A liquid crystal display apparatus according to claim 1, wherein said display data holding circuit includes a thin film transistor which has a gate connected to the corresponding scanning electrode and one of a drain and a source connected to corresponding signal electrode, and a static memory circuit connected to the other of the drain and the source of said thin film transistor, the static memory circuit including a plurality of thin film transistors.

10. (amended) A liquid crystal display apparatus having a pair of substrates of which at least one substrate is transparent and a liquid crystal layer sandwiched between the substrates, comprising:

a plurality of first scanning electrodes formed on one of the substrates;

a plurality of signal electrodes intersecting in a matrix form with said plurality of first scanning electrodes;

a plurality of second scanning electrodes provided along said first scanning electrodes or said signal electrodes;

wherein the display apparatus further comprises, within each of the regions surrounded by said plurality of first scanning electrodes and said plurality of signal electrodes:

(a) a data holding circuit connected to a corresponding first scanning electrode, signal electrode, and second scanning electrode for fetching and storing

display data from the signal electrode in response to voltages applied to the first and the second scanning electrodes;

(b) a capacitor connected to said data holding circuit;

(c) a switching device connected to said capacitor and having a switching operation thereof controlled by a voltage of the capacitor; and

(d) a display electrode connected to said switching device;

wherein a drive voltage of the liquid crystal display apparatus is an alternating current voltage having a period which is shorter than a period of fetching by the display data holding circuit.

11. (amended) A liquid crystal display apparatus according to Claim 10, wherein said switching device for driving pixels is composed of a TFT device: a signal for switching operation is input to a gate terminal of said TFT device, a drain terminal of said TFT device is connected to a display electrode, and a source terminal is connected to a reference line defining an average voltage of a liquid crystal drive voltage; and including AC voltage generation means for generating ~~a~~ the liquid crystal drive voltage and timing signal generation means for generating a timing signal which is synchronized with a time when said liquid crystal drive voltage generated by said AC voltage generation means reaches an average voltage.

Please cancel claims 12 and 13 without prejudice or disclaimer of the subject matter thereof.

Please amend claim 14 as follows:

14. (amended) A liquid crystal display apparatus according to claim ~~11~~ 10, wherein each of said data holding circuits comprises:

a first thin film transistor connected to a corresponding first scanning line at a gate thereof and to a corresponding second scanning line at one of a drain and a source thereof; and

a second thin film transistor connected to a corresponding signal electrode at a gate thereof and connected with said first thin film transistor and said capacitor in series.

Please cancel claims 15-17 without prejudice or disclaimer of the subject matter thereof.

Please add the following new claims:

--18. A liquid crystal display apparatus having a pair of substrates of which at least one substrate is transparent and a liquid crystal layer sandwiched between the substrates, comprising:

a plurality of scanning electrodes formed on one of the substrates; and

a plurality of signal electrodes intersecting in a matrix form with said plurality of scanning electrodes;

wherein the display apparatus further comprises, within each of the regions surrounded by said plurality of scanning electrodes and said plurality of signal electrodes:

(a) a display data holding circuit having one of an inverse stagger structure and a coplanar structure, and connected to a corresponding scanning electrode and signal electrode, for fetching and storing display data from a signal electrode in response to a scanning signal for holding a display image without updating the display data while a power supply to the display apparatus is maintained, said power supply applying an alternating current voltage;

(b) a switching device connected to said display data holding circuit and having a switching operation thereof controlled by the display data holding circuit, said switching device including a first switching device controlling connection and disconnection between a first electrode applied an alternating current voltage having the same phase as said power supply and a display electrode, and a second

switching device connecting and disconnecting between a reference electrode applying a reference voltage to the display electrode, and said display electrode; and

(c) a display electrode connected to said switching device, said first and second switching devices being controlled so that only one of said first and second switching devices is turned ON depending upon the digital display data stored in said display data holding circuit.

19. A liquid crystal apparatus according to claim 18, wherein a control of said second switching device in each period of an alternating current voltage applied to the power supply provides a first period and a second period substantially immediately before reversal of polarity of said alternating current voltage, and further comprising:

a second pixel enabling driving of a voltage waveform applied to the display electrode having polarity substantially inverted to that of said alternating current voltage waveform by controlling based on the digital display data in said first period and controlling to be in an OFF condition irrespective of the display data in said second period;

a first pixel enabling driving so as to constantly apply said alternating current voltage to said display electrode when said switching device is in an ON condition by constantly controlling said second switching device based on the display data and driving only one of said first and second switching devices to be in the ON condition;

wherein said first pixels and said second pixels are arranged alternately for inverting polarities of the liquid crystal driving voltage of adjacent pixels.

20. A liquid crystal display apparatus according to claim 19, wherein said second switching device is constructed with one of a coplanar and inverse stagger TFT, a gate electrode thereof is connected to said data holding circuit and said reference voltage via a first control TFT and a second control TFT;

said first control TFT and said second control TFT are constructed with mutually different types of TFT of pch and nch, and gate terminal thereof is connected to the control line.

21. A liquid crystal display apparatus according to claim 18, wherein said display electrode is an opaque reflection electrode arranged in overlapping relationship with at least one of said scanning electrode, said signal electrode and a thin film transistor for enabling driving of the liquid crystal display apparatus in a reflection type display mode.

22. A liquid crystal display apparatus according to claim 21, wherein said liquid crystal layer is a guest-host type liquid crystal.

23. A liquid crystal display apparatus according to claim 1, wherein said display electrode is an opaque reflection electrode arranged in overlapping relationship with at least one of said scanning electrode, said signal electrode and a thin film transistor for enabling driving of the liquid crystal display apparatus in a reflection type display mode.

24. A liquid crystal display apparatus according to claim 23, wherein said liquid crystal layer is a guest-host type liquid crystal.

25. A liquid crystal display apparatus according to claim 10, wherein said display electrode is an opaque reflection electrode arranged in overlapping relationship with at least one of said scanning electrode, said signal electrode and a thin film transistor for enabling driving of the liquid crystal display apparatus in a reflection type display mode.

26. A liquid crystal display apparatus according to claim 25, wherein said liquid crystal layer is a guest-host type liquid crystal.--